33.3 Dual-band Single-Ended-Input Direct-Conversion DVB-H Receiver

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DVB-H is a new standard that is expected to be widely deployed in future mobile devices. The first DVB-H field trials were held in Europe and used the UHF band. Since then, DVB-H has also been targeted for deployment in the United States using L-band spectrum between 1670MHz and 1675MHz. There has also been discussion of reallocating European L-band DAB frequencies for DVB-H service. In this paper, a dual-band DVB-H tuner, designed to cover UHF band IV, V, and L-band applications, is presented.

During the initial phase of UHF DVB-H deployment, it is expected that the existing DVB-T infrastructure will be leveraged. DVB-H receivers require a lower NF than stationary antenna DVB-T systems that take advantage of line-of-sight reception [1]. The mobile nature of DVB-H receivers requires that components be small and the consumer markets require that they be inexpensive. Previous published work relied on a 2-chip solution with an external balun for single-ended to differential conversion [2]. The presented solution is a single chip that eliminates the need for an external LNA and balun.

The architecture of the receiver is shown in Fig. 33.3.1. The RF signal is routed to one of the three parallel cascode LNAs. The frequency band and the signal power determine the active LNA. For weak signals in the UHF band, a fixed-gain UHF LNA is available. For stronger signals, a similar LNA with a resistive divider input attenuator is selectable. This LNA maintains its OIP3 over the gain range at the expense of higher NF. The L-band LNA has a parallel LC load to provide a low NF and high gain at the resonant frequency.

The receiver has 2 direct-conversion mixers to generate baseband quadrature signals. The mixer transconductance stage is shown in Fig. 33.3.2. To facilitate connection to the single-ended LNAs, each mixer has a single-ended voltage input and provides differential current outputs. Signals from the L-band and UHF paths are converted to differential currents by the differential pairs formed by Q1, Q2, and Q3. The mixer is the only device in the signal path that has to cover the entire frequency range from 470MHz to 1900MHz. The low-frequency operation requires a large capacitor to be connected to the base of Q3. An external capacitor is chosen because it is more cost effective. The differential currents are folded into the emitters of the mixing quad current sources Q4 and Q5 creating a low impedance at the collectors of the differential pairs. This low impedance provides several advantages. First, it minimizes the voltage swing at the collectors of Q1, Q2, and Q3 preventing saturation and allowing low voltage operation. Second, the low impedance helps extend the frequency range. Third, it reduces distortion contribution due to voltage modulation of the nonlinear collector-base capacitance. Fourth, LO-RF isolation is improved because Q4 and Q5 isolate the differential pairs from the mixing quad.

The baseband anti-aliasing and channel selection filter is a 7^{th}-order Chebyshev type II filter with 80dB stopband attenuation. With this attenuation, interferers with undesired-to-desired ratios of up to 50dB can be tolerated. This filter topology provides a flat passband response with relatively low-Q poles and low group-delay variation. The filter uses a three-opamp biquad implementation [3] to minimize I/Q channel mismatch due to component matching errors. Layout symmetry and feature sizes are optimized in the filters and mixers to improve I/Q matching and reduce static dc offsets.

Static and dynamic dc-offset correction (DCOC) is implemented by a LPF placed around the first two baseband biquad filters. Low-pass filtering in the feedback path causes high-pass filtering in the overall closed loop, thereby rejecting dc offsets. The summation point is current-mode and differential, thus the DCOC consists of a differential transconductance and passive RC filter for each I and Q path. The high-pass pole at 300Hz removes only one OFDM subcarrier even with a channel BW of 5MHz in the 8k mode.

The fractional-N frequency synthesizer consisting of VCOs, dividers, phase detector, and charge pump is shown in Fig. 33.3.3. It covers the frequency range from 470MHz to 1900MHz and uses two different frequency planning schemes for UHF and L-band. The quadrature outputs are generated by 2 CML divide-by-2 FFs triggered by opposite clock edges. Two fully integrated differential LC oscillators cover the entire frequency range. The PLL uses coarse digital and fine analog tuning. The VCOs are operated at multiples of the RF frequency to allow higher Q-factors for the integrated inductors as well as to facilitate I/Q generation by divide-by-2 circuits. The loop filter is realized with off-chip discrete components and has a loop bandwidth of approximately 30kHz. A typical phase noise plot for the UHF band at 612MHz is shown in Fig. 33.3.4.

Some key chip parameters are listed in Fig. 33.3.5 for both the UHF and the US L-band. Although the L-band numbers are quoted for the range from 1670 to 1675MHz, the L-band signal path can be tuned via component selection to any narrow band within the L-band. The gain range is composed of 30dB of baseband AGC range plus LNA range. Sensitivity is measured with a 16-QAM modulated signal. The quoted UHF phase noise numbers are typical results over the frequency range. The performance complies with the MBRAI test cases [4]. Figure 33.3.6 shows a 16-QAM measurement with 8MHz BW and code rate (CR) of $^{2}/_{3}$ at the upper UHF band and is representative of the performance achieved over the whole UHF and L-band ranges. The power consumption is 340mW, which is comparable to the power consumption of the previously published 2 chip solution when the power consumption of the external LNA is included [2]. The micrograph of the 12.25mm^2 die is shown in Fig. 33.3.7. For L-band operation, the extra circuitry is mainly in the LNA section, which only accounts for a small fraction of the overall die area.

Acknowledgement:
The authors thank David Dessert, Mark Appel, Rudolf Manhart, and Shih-Lin Lu for their measurement support and Kirk Ashby for his editorial advice.

References:
[1] A. Bria, D. Gómez-Barquero, "Scalability of DVB-H Deployment on Existing Wireless Infrastructure," *IEEE PIMRC Symposium*, Sept., 2005.
[2] P. Antoine et al., "A Direct-Conversion Receiver for DVB-H," *ISSCC Dig. Tech. Papers*, pp. 426-427, Feb., 2005.
[3] E. J. Kennedy, Operational Amplifier Circuits, 1st Ed., Holt, Rinehart and Winston, 1988.
[4] Mobile and Portable DVB-T Radio Access Interface Specification, European Industry Association EICTA, MBRAI-02-16, Version 1.0, 2003.

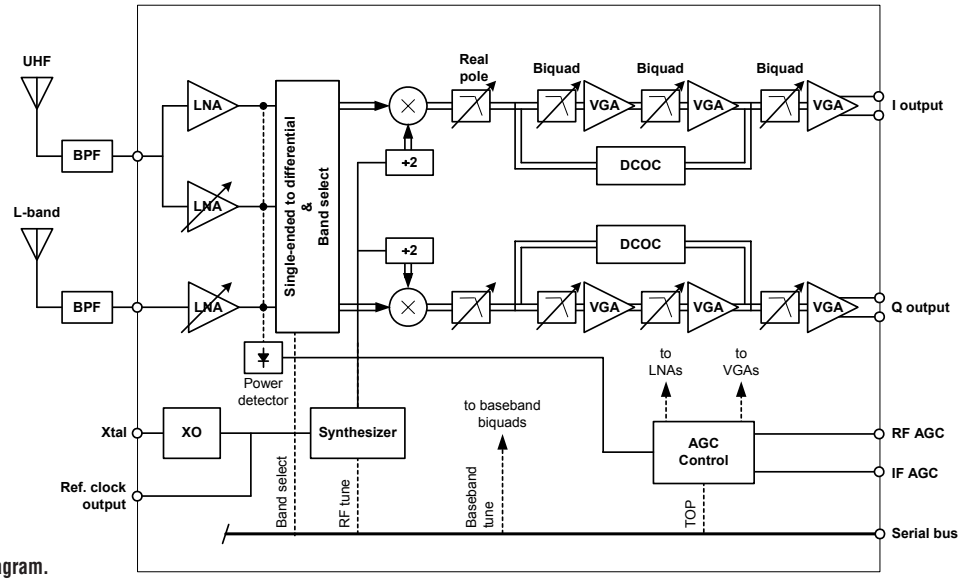

Figure 33.3.1: IC block diagram.

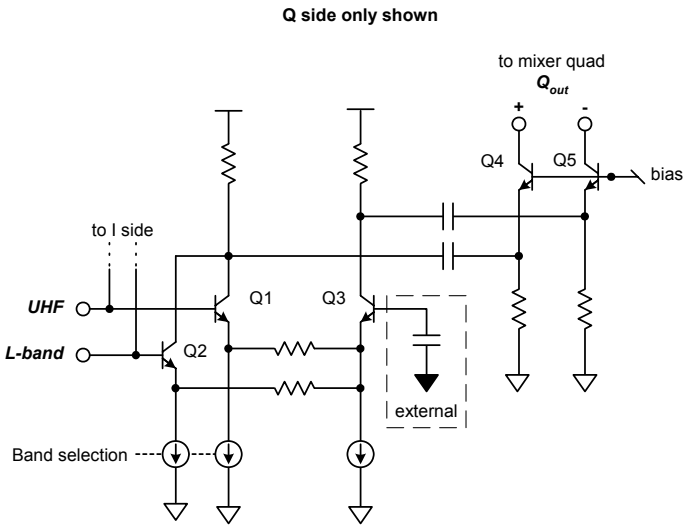

Figure 33.3.2: Mixer transconductance stage.

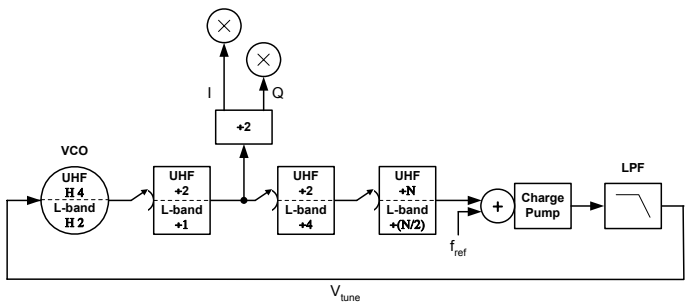

Figure 33.3.3: Synthesizer block diagram.

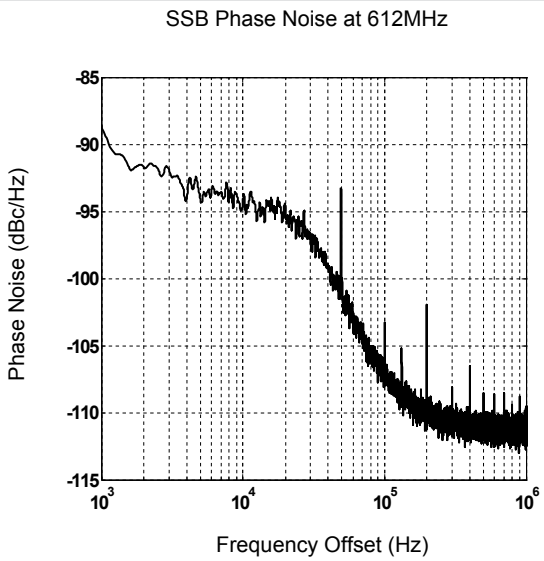

Figure 33.3.4: Phase noise plot.

Frequency range	UHF 470 - 862MHz	L-band 1670 - 1675MHz
Maximum gain	85dB	80dB
Gain range	65dB	60dB
NF @ max gain	3.6dB	3.5dB
Sensitivity (16 QAM, $CR^2/_3$, BW 8MHz)	-89dBm	-88dBm
IIP3 @ 20dB RF attenuation	4dBm	8dBm
IIP2 @ 20dB RF attenuation	>27dBm	not applicable
LO phase noise		
1kHz	-86dBc	-80dBc
10kHz	-87dBc	-87dBc
100kHz	-106dBc	-104dBc
Channel bandwidth	7 or 8MHz	
Stop band attenuation	80dBc	
I/Q matching	-35dBc	
Power consumption	340mW (100% duty cycle, max. linearity mode)	
Supply voltage	2.7V	
Die size	3.5mmx3.5mm	
Technology	0.35µm SiGe BiCMOS	

Figure 33.3.5: Performance summary.

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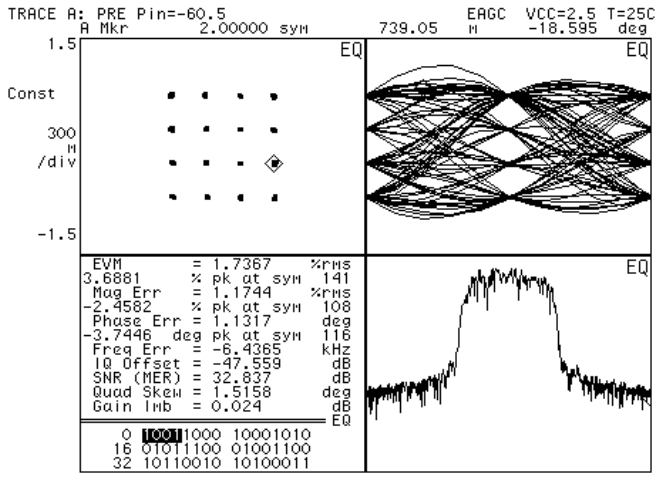

Figure 33.3.6: 16-QAM measurement.

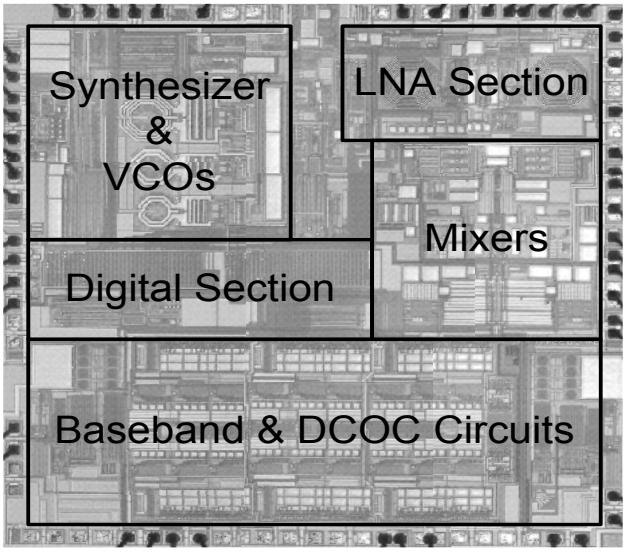

Figure 33.3.7: Die micrograph.

